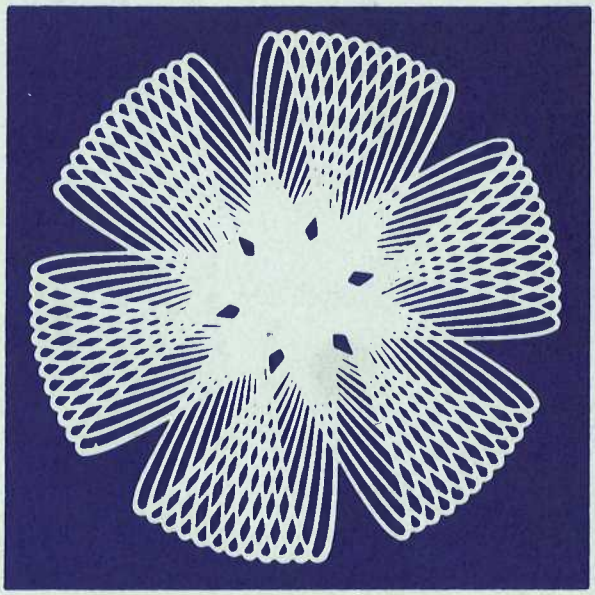
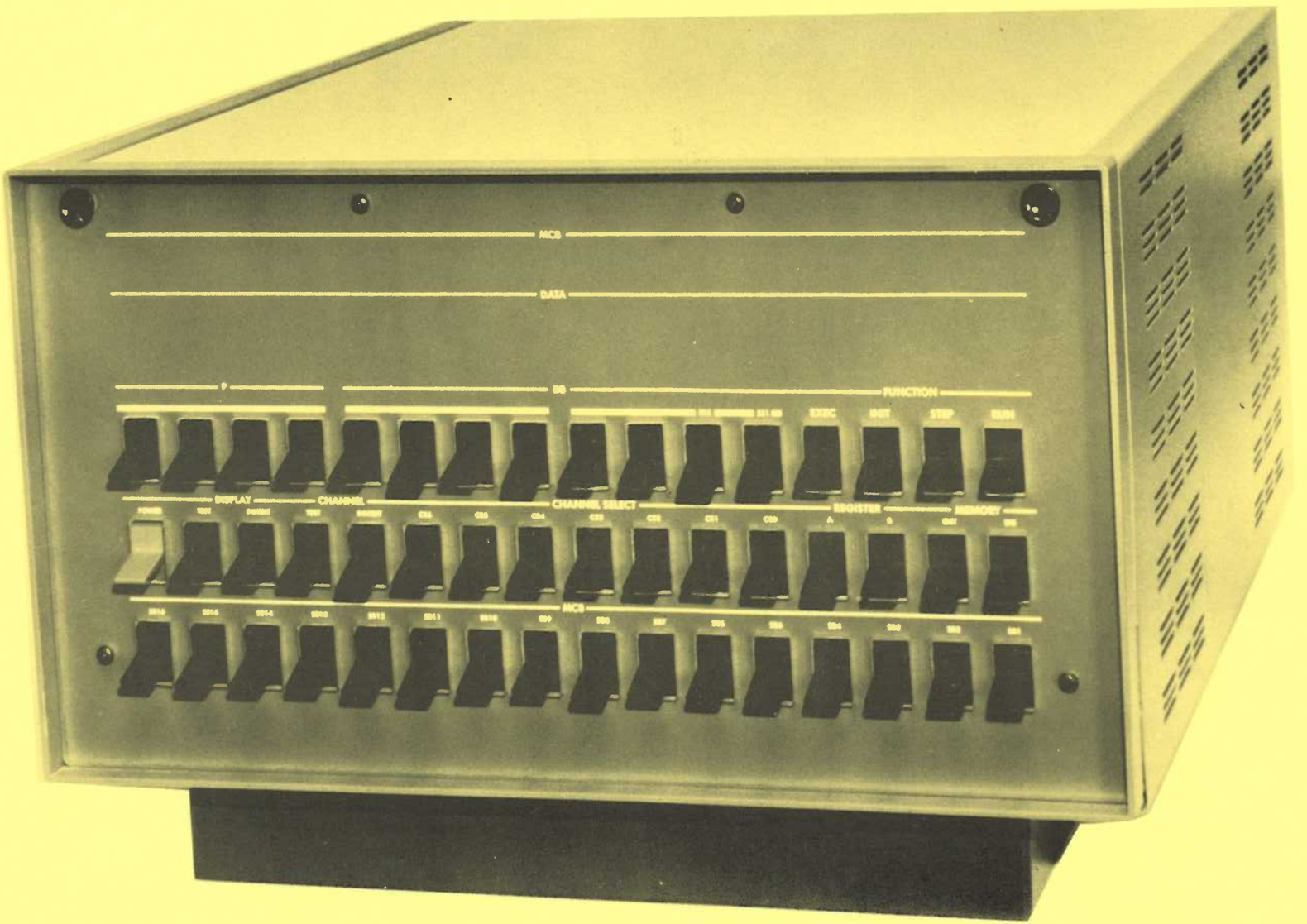
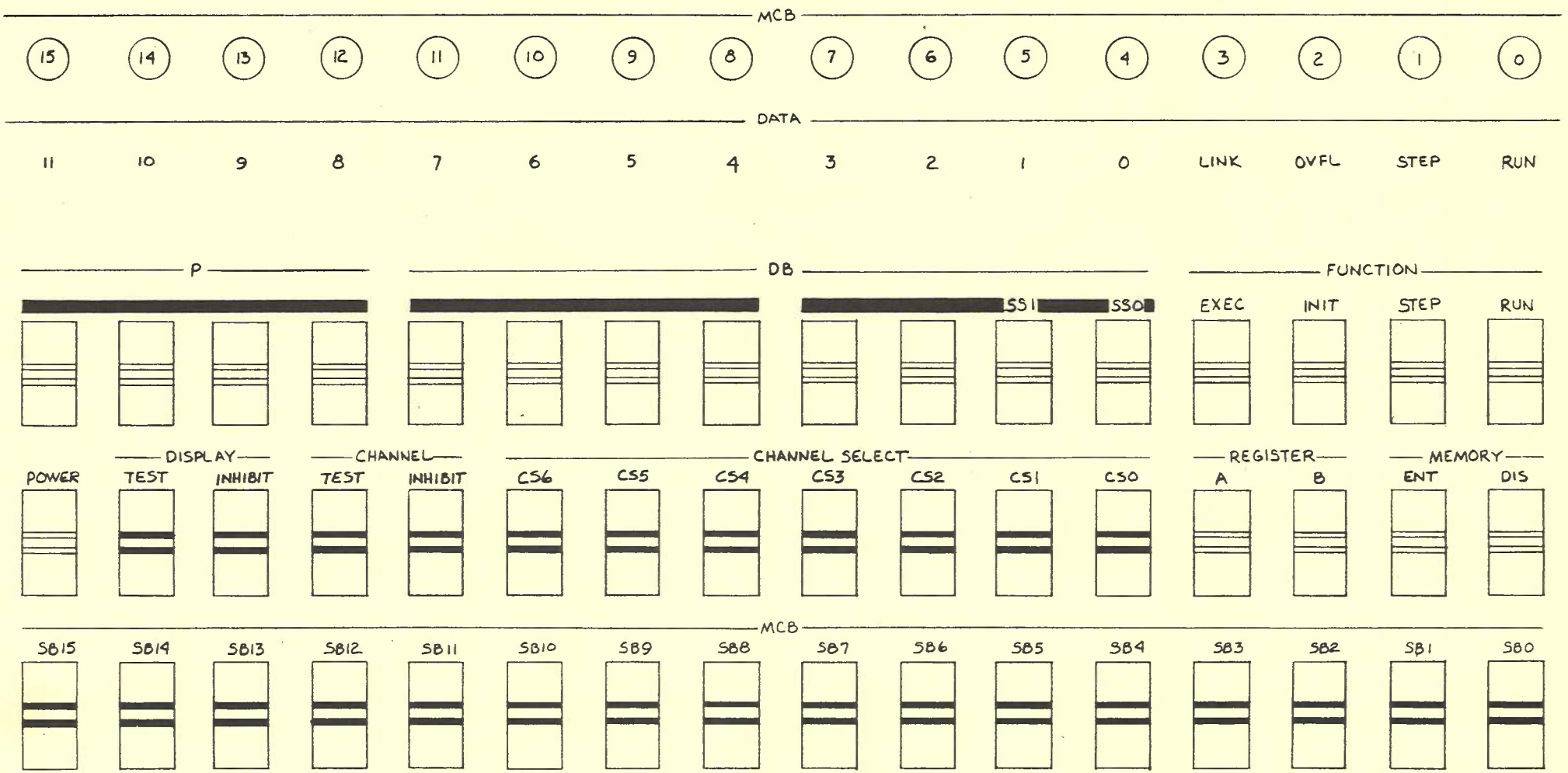
COMSTAR



STAR SYSTEM

7413 WASHINGTON AVE. SO., EDINA, MINN.■612-941-4454


MCR
DATA
P
SR
FUNCTION
EXEC
SHIFT
STEP
RUN
DISPLAY
CHANNEL
CHANNEL SELECT
REGISTER
MEMORY
A
B
MCR


MCB
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
DATA
11 10 9 8 7 6 5 4 3 2 1 0 LINK OVFL STEP RUN
P
DB
SS1
SS0
FUNCTION
EXEC INIT STEP RUN
DISPLAY
CHANNEL
CHANNEL SELECT
REGISTER
MEMORY
POWER TEST INHIBIT TEST INHIBIT CS6 CS5 CS4 CS3 CS2 CS1 CS0 A B ENT DIS
MCB
SB15 SB14 SB13 SB12 SB11 SB10 SB9 SB8 SB7 SB6 SB5 SB4 SB3 SB2 SB1 SB0

Star System I Control Process Unit

-Hardware Brief-

The Star System I Control Process Unit is a low price, high performance, general purpose minicomputer. The extensive use of MSI circuitry combined with automated manufacturing provides the user with a remarkable powerful instrument at a very low price. Basic design considerations were given to optimizing the processor for applications to such tasks as peripheral control, data communications, instrumentation, process control, and automatic testing. With excellent computation ability, easy interfacing, and modular design the Star System I CPU is truly a systems component.

Possessing a flexible programming capability and high speed hardware (1.6 microseconds) this minicomputer is designed to interconnect with other elements in the control system with unique simplicity and low cost.

The Star System I CPU features multi-register architecture organization for general purpose controller applications. The machine has 99 basic instructions and 74 optional instructions. The memory modification instructions are powerful in bit manipulation, counting and control routines.

Memory is expandable from a basic 4,096 words of core memory to 65,536 words of core memory in increments of 4K per memory board. This unit is the only computer in its class and price range to employ base register addressing. This provides the capability to directly address 65,536 words of memory. The base register addressing feature provides the user with total program relocatability

A problem oriented Process Control Language (PCL) is provided for use with the Star System I CPU unit to solve a major problem in the application of minicomputers. Assembly languages which are usually provided with the typical minicomputer have in the past demanded sophisticated programming support. Compace Controls provides

the user with a Process Control Language tailored for applications at the macro level. PCL frees the Process Engineer from repititious subroutine programming and instead provides a repertoire of problem oriented instructions specifically designed for the job.

Star System I Control Panel

-Hardware Brief-

The Control Panel of the Star System I Unit is composed of 32 indicator lights and 48 switches designed to assist the Process Engineer in the operation, maintenance, and testing of his entire control system. Two different and independent functions are performed by two groups of switches and indicators. The first group controls the operation of the CPU itself and is composed of:

(1) the lower level of indicator lights,

(2) the top layer of switches, and

(3) the power, register, and memory switches in the middle row of switches.

The second group of switches and indicators is used in the maintenance and testing of all equipment in the process control system. This group includes:

(1) the top layer of indicator lights,

(2) the bottom row of switches, and

(3) the display and channel switches in the middle layer of switches.

I

This section documents in general the use of Group I switches and indicators. The indicators in the upper right section display control conditions, while the indicators directly above the data switches display the accumulators, memory data or the program counter. The data switches can best be visualized as a hardware register through which the operator can supply addresses and data to the processor. The UP position of the data switch represents a one. The four switches on the right side of the operator's panel (EXC, STEP, INIT, RUN) are momentary contact spring return switches. They provide control signals to initiate action in the central processor. All register and memory entry or display must be performed in the step mode. All switches except step and data entry switches zero and one, which are used as sense switches, are interlocked so they have no effect in the run mode.

INDICATORS

When any indicator is lit, the associated function is in the true (1) state. The indicators can display useful information in the run mode but most can change too rapidly to be valid. They are therefore discussed in terms of information displayed in the step mode. There are 16 indicators in the Group I section of the Star System I Control Panel. The eight Data Bit (DB) indicators display the contents of the selected register; A, B, P, or Memory Data. The four P indicators display the upper four bits of the P register in conjunction with the DB indicators displaying the low order eight bits. The P indicators are only lit when P is selected for display. The control conditions OVFL (overflow), Link, Step and Run are also displayed.

SWITCHES

REGISTER SELECT

The A, B, P, and MD registers can be controlled from the control panel. The P register is displayed when the A. B. Memory Enter and Memory Display switches are in the off (down) position. The front panel data switch contents can then be transferred to the P register by raising the EXC switch. The A, B or Memory Data register can be selected by raising the respective switch. When the A or B register is selected, the contents of that register are displayed. When Memory ENT or Memory DIS are selected, the contents of the Memory Data register are displayed. Except for Memory DIS, the data switch contents can be transferred to the selected register by raising the EXC switch. With Memory DIS selected, the contents of the memory cell addressed by the program counter will be displayed by raising the EXC switch.

DATA ENTRY SWITCHES

Eight alternate action switches are used to enter data into the selected register or into memory. Four additional switches are associated with the upper 4-bits of the P register. Data Entry Switches zero and one also serve as sense switches in the run mode.

MEMORY SELECT

The contents of memory can be displayed or altered from the front panel. The address of the memory location is loaded into the P register. When ENT is selected and the EXC switch is raised, the contents of P will be strobed into the memory address (MA) register and the contents of the eight data switches will be strobed into the memory data (MD) register and stored in core. When DIS is selected and the EXC switch is momentarily raised, the contents of P are transferred to the MA register and the memory data contained in that location is strobed into the MD

register and displayed on the control panel.

STEP

When the computer is in step mode and neither the memory of register select switches are selected, raising the step switch will cause the next instruction (as addressed by P register) to be executed. When the computer is in the run mode, raising the STEP switch will cause the computer to enter the step mode. The STEP switch will also perform an increment P if either the memory DIS or memory ENT switches are selected. The STEP switch increments P without executing instructions as long as either the ENT or DIS memory switch is selected, therefore when successive addresses are to be displayed or altered, the STEP switch can be used.

RUN

If the memory ENT or DIS switches are not selected and the computer is in the STEP mode, momentarily raising the RUN switch will cause the computer to enter the RUN mode.

INIT (Initialize)

The INIT is functional only in the STEP mode and is used to initialize the computer and external devices.

POWER

The power on/off switch controls the relay that switches AC to the power supply and AC sequencer.

SS1 AND SS2 SENSE SWITCHES

The SS1, SS2, and STEP switches are the only switches active in the RUN mode. In the STEP mode, during data entry operations, the SS1 and SS2 switches are data switches bit 0 and 1. In stepping through a program or in the RUN mode, they are used as sense switches, and are interrogated by the SKIP commands to cause breakpoint or branching of a control program.

II

This section documents in general the use of Group II switches and indicators. If all parts of the control system are functioning satisfactorily Group II switches and indicators are not used by the Process Engineer. Should a problem in the control system arise Group II switches and indicators allow the Process Engineer to pinpoint the source of difficulty and its remedy rapidly. This capability is extremely valuable:

(1) in the initial debugging of the control system,

(2) in checking line equipment,

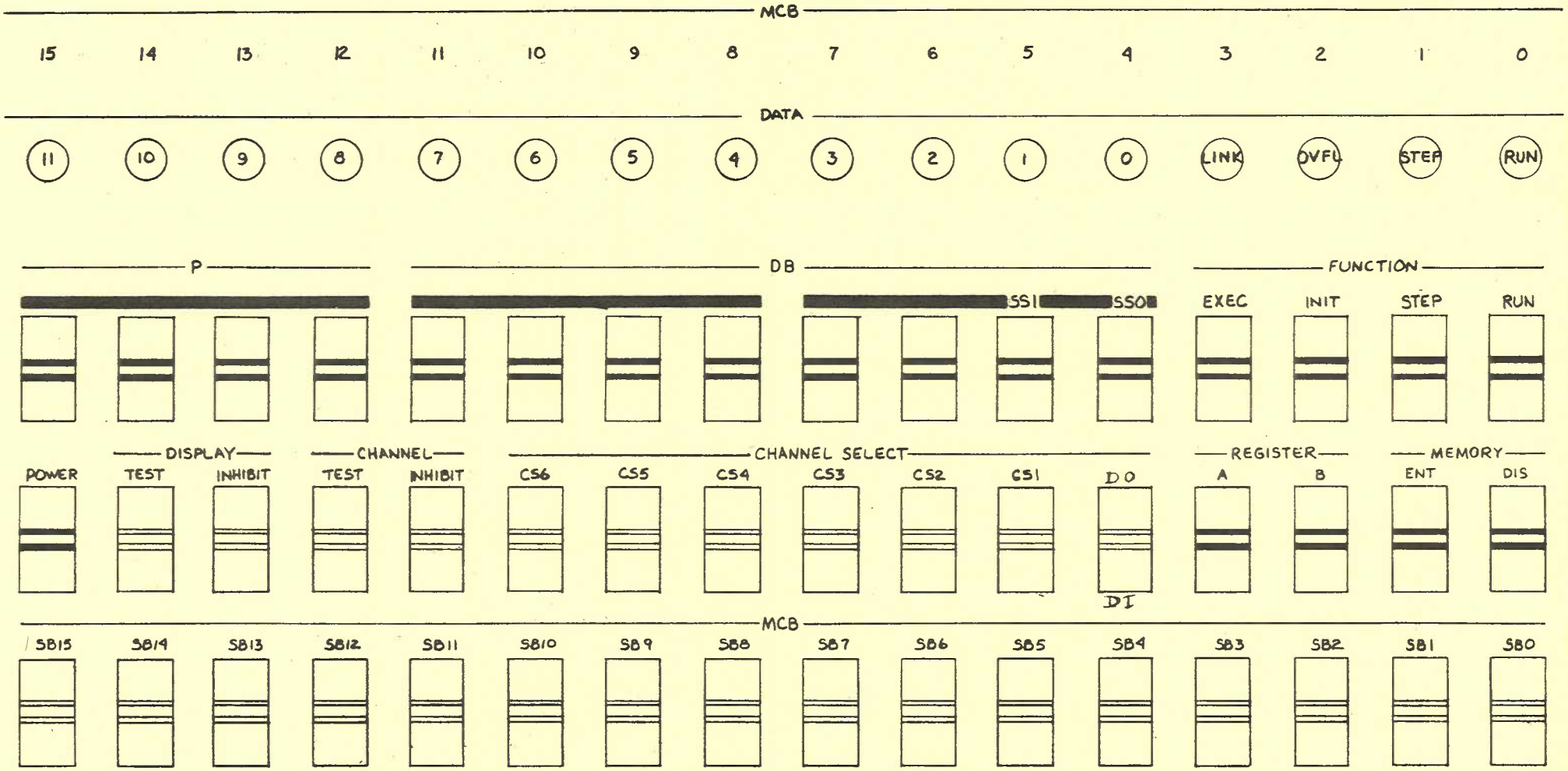
(3) in testing the program in the CPU,

(4) in troubleshooting,

(5) in executing a specific controlled action, and

(6) in monitoring troublespots in the control process.

All of these possible functions make Group II switches and indicators an important part of Star System I.


MCB
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
DATA
11 10 9 8 7 6 5 4 3 2 1 0 LINK OVFL STEP RUN
P
DB
SS1
SS0
FUNCTION
EXEC INIT STEP RUN
DISPLAY
CHANNEL
CHANNEL SELECT
REGISTER
MEMORY
POWER TEST INHIBIT TEST INHIBIT CS6 CS5 CS4 CS3 CS2 CS1 DO A B ENT DIS
DI
MCB
SB15 SB14 SB13 SB12 SB11 SB10 SB9 SB8 SB7 SB6 SB5 SB4 SB3 SB2 SB1 SB0

CHANNEL SELECT

These seven switches allow the Operator to select the particular digital input or output channel he wishes to examine. Since all channels are given a seven digit binary address these switches are capable of selecting any one channel from the 118 available. Basically each digital module consists of sixteen digital input or output bits. These sixteen bits are divided into two groups of eight bits called channels, therefore, one digital module consists of two channels and has two unique channel address select codes; i.e. one for each channel. However, when a channel is to be selected for test, using the CS switches, both channels on the digital module will be selected because address bit O is not used. For example, if the Operator wants to investigate Input Channel #53 (decimal) he sets the Channel Select switches to the binary address which corresponds to #53. In this example the address would be 011010 and the Operator would place Channel Select switches 2, 4, and 5 in the Up position and switches 1, 3, and 6 in the DOWN position. He is now prepared to display and test Channel #53.

MCB (Multiplexer Channel Bit)

Since each digital module is composed of sixteen bits, this bottom row of switches allows the Operator to define and control the state of any or all bits in the selected channel.

DO - DI SELECT

Since a Digital Input (DI) and a Digital Output (DO) module can have the same channel select address, this switch will select only the module desired.

DISPLAY CAPABILITY

The Display Inhibit and Display Test switches allow the Operator to visually monitor the contents of a selected channel.

1. When the Display Inhibit switch is in the UP position the display lights on the top row are inhibited and will not light. The Display Test switch is also disabled and has no function.

2. When the Display Inhibit switch is in the DOWN position and the Display Test switch is DOWN the MCB indicator lights will display the contents of the selected channel. The Operator can thus monitor the operation of a DI or DO channel without disturbing the operation of the total system. He can also monitor the effects of his tests when troubleshooting in the system, see Channel Control Capability.

3. When the Display Inhibit switch is DOWN and the Display Test switch is UP all 16 MCB indicator lights should go on. If they do not there is a malfunction in the display logic of the selected channel or an indicator light is burned out. In effect this operation preforms a lamp test.

CHANNEL CONTROL CAPABILITY

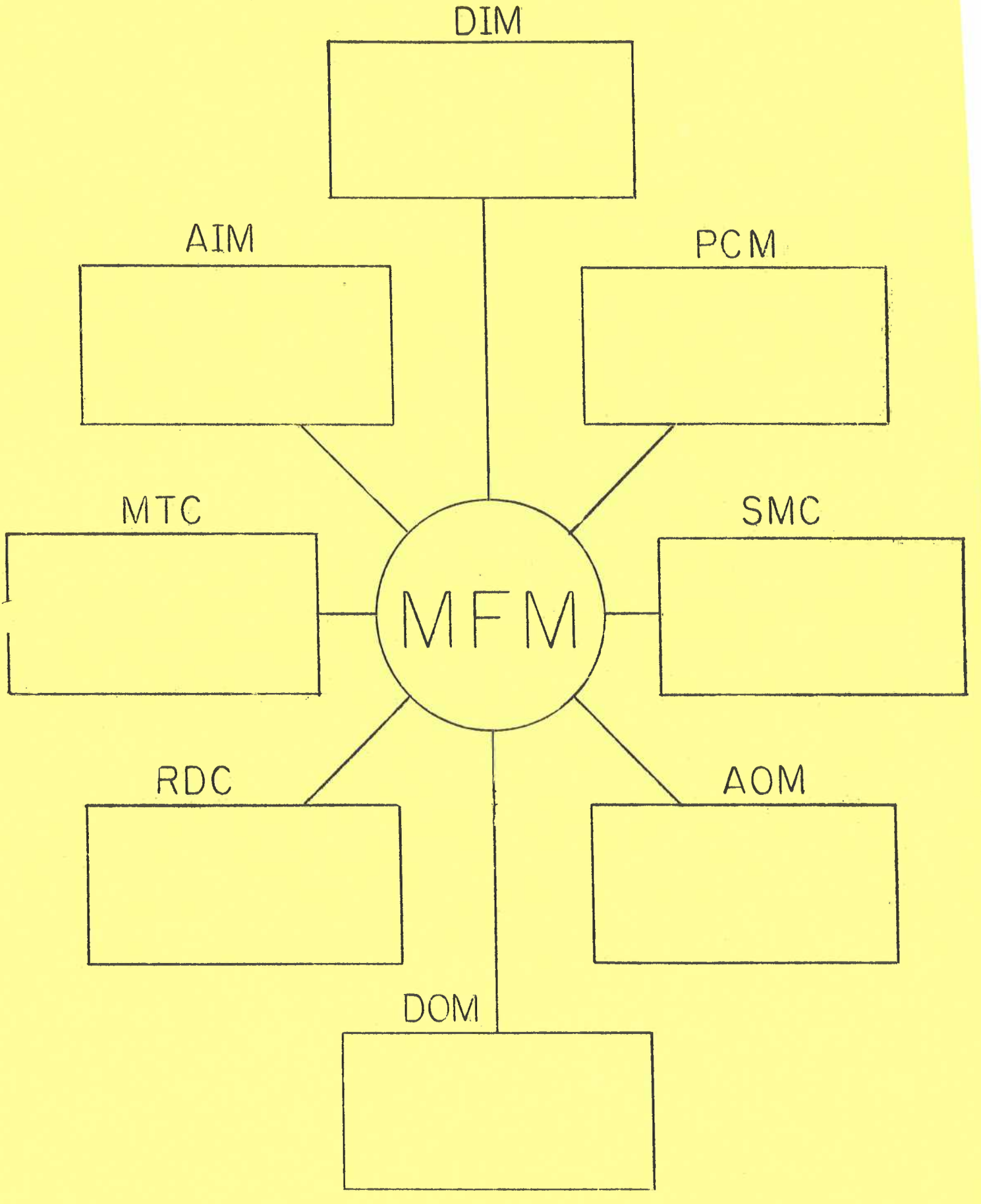
By using the Channel Test, Channel Inhibit, and MCB switches, the Operator can alter the bit pattern of a selected channel.

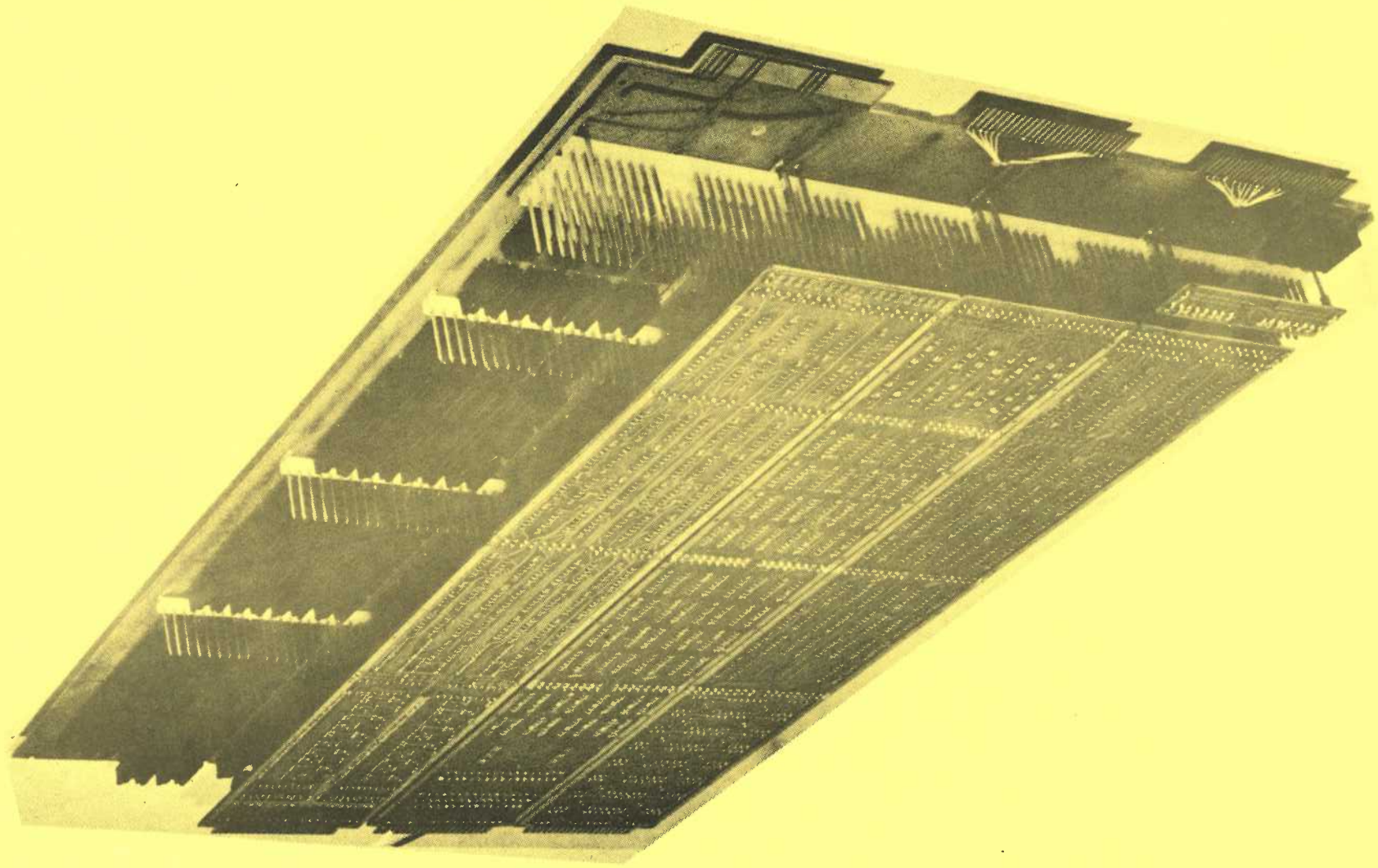
1. With the Channel Inhibit and Channel Test switches in the DOWN position the selected channel will continue to operate normally regardless of the position of the MCB switches. This condition would be the normal state of a satisfactorily functioning Star System.

2. With the Channel Inhibit switch UP and the Channel Test switch DOWN the Operator can force LO (or 0) any or all bits in the selected channel simply by putting the corresponding MCB switches in an UP position. For example, the Operator can define bits 7, 10, and 11 in a selected channel by placing MCB switches 7, 10, and 11 in an UP position. He then knows that these bits are forced into a 0 (or LO) condition regardless of whether they were in a O or 1 (i.e. LO or HI) condition before this action.

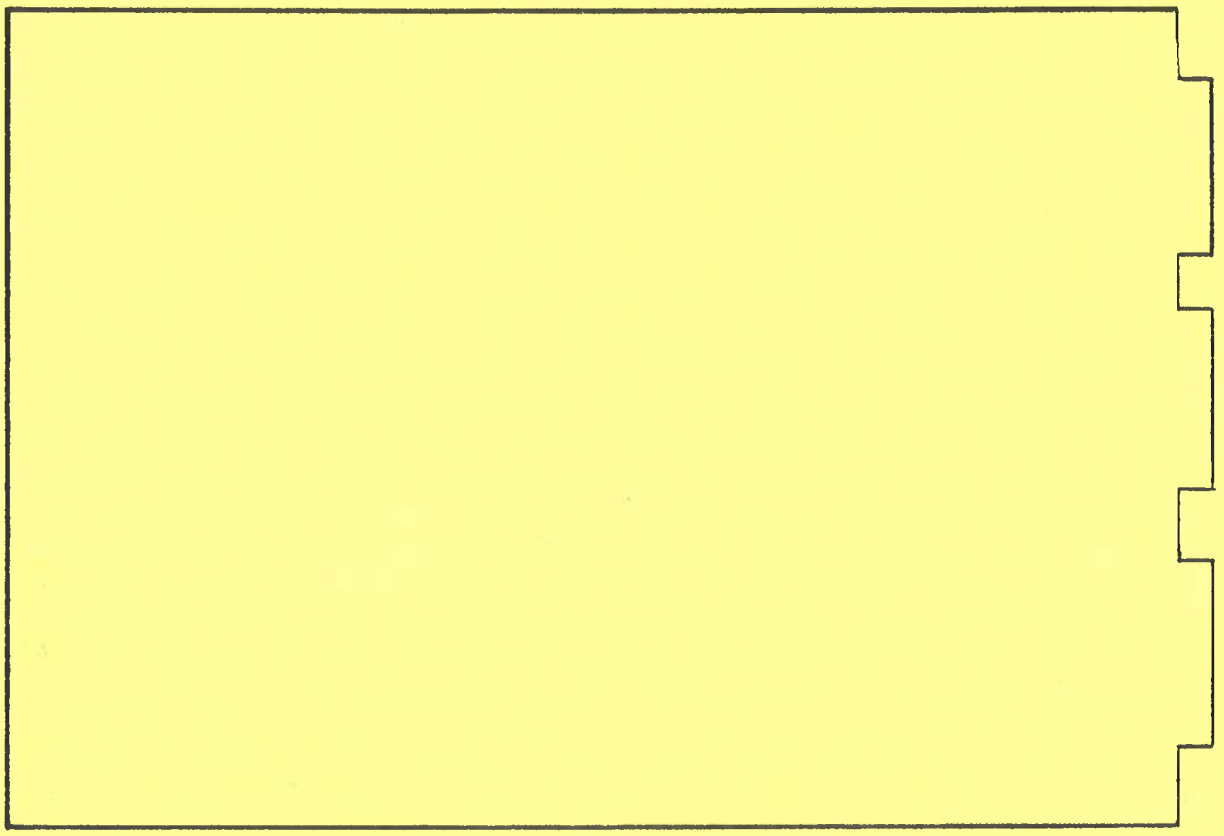
3. With the Channel Inhibit switch DOWN and the Channel Test switch UP the Operator can force HI (or 1) any or all bits in the selected channel simply by putting the corresponding MCB switches in an UP position. For example, the Operator can define bits 1, 3, 9, and 13 in a selected channel by placing MCB switches 1, 3, 9, and 13 in an UP position. He then knows that these bits are forced into a 1 (or HI) condition regardless of whether they were in a 0 or 1 (i.e. LO or HI) condition before this action.

Equipped with this control capability the Operator can manually check all field devices in the control system and all internal control logic. In effect the entire Star System I control Process can be examined and monitored from the central Control Panel.


DIM
AIM
PCM
MTC
MFM
SMC
RDC
AOM
DOM



MULTIFUNCTIONAL MODULE



FEATURES:

- UP TO 16 MFM's CAN BE CONNECTED TO AN I/O CHANNEL
- UP TO 4 FM's CAN BE CONNECTED TO A MFM
- PROVIDES INTERRUPT PRIORITY BY POSITION TO THE I/O CHANNEL
- PROVIDES INTERCHANGEABLE ADDRESS SELECTION BLOCKS FOR FM's
- PROVIDES CONTROL SIGNALS TO THE FM's FROM THE PROCESSOR
- PROVIDES STATUS SIGNALS TO THE PROCESSOR FROM THE FM's
- INCLUDES TEST AND DISPLAY LINES FOR MANUAL CONTROL AND MONITORING OF FM's

Multifunctional Module

-Hardware Brief-

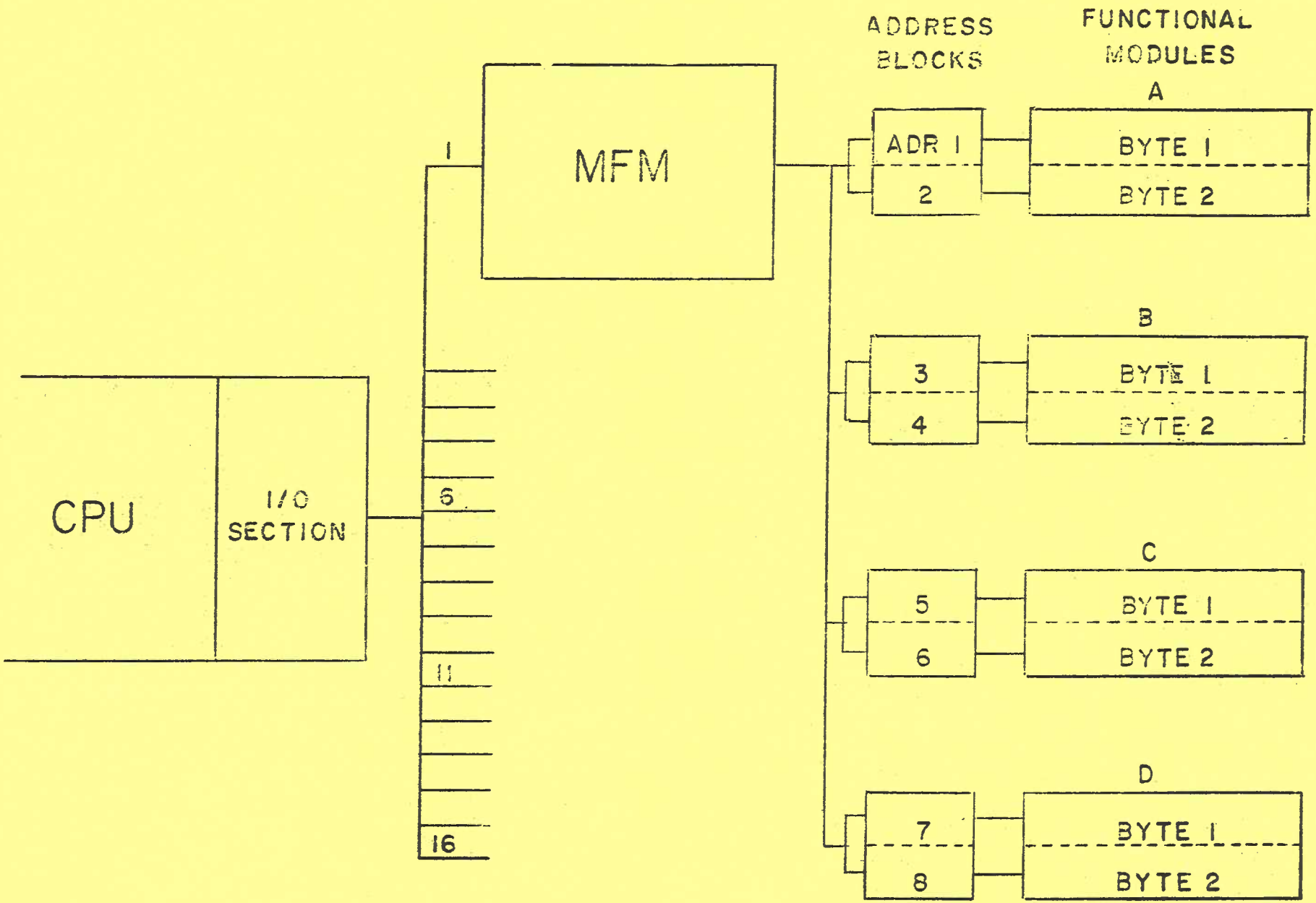
The Multifunctional Module (MFM) is basically a mother board for the eight Star System Functional Module (FM) daughter boards. Up to 16 MFM's can be connected to a Star System CPU and up to 4 FM's can be connected to a single MFM. Thus a total of 64 FM's can be used in a maximum Star System configuration.

Each Functional Module is assigned an address block which contains two seven bit addresses. The total address capability of the Star System is thus 128 (or 2^7) addresses. Each FM is given two addresses because each is treated as handling two 8-bit bytes. All address blocks are daughter boards to the MFM and can be interchanged as required.

The flexible and modular design of the MFM-address block-FM chain allows for an unusually adaptable and expandable process control system. The modular design of the eight Star System FM's allows their easy application to analog and digital devices in addition to local and remote peripherals.

The MFM uses a bus organization that allows direct access between the CPU and a FM , via the MFM, when a FM is selected by the CPU. The MFM also allows a FM to interrupt the CPU on a priority basis with the first FM in the system assigned the highest priority. The CPU has the capability of inhibiting a FM interrupt if it is not required.

During data/status transfers the MFM will demultiplex the FM address selected by the CPU and allow the data/status from the selected FM to be transmitted to or from the CPU. In addition the MFM has a test and display bus to allow manual control and monitoring of FM's and a 5MHZ clock signal for FM timing needs.

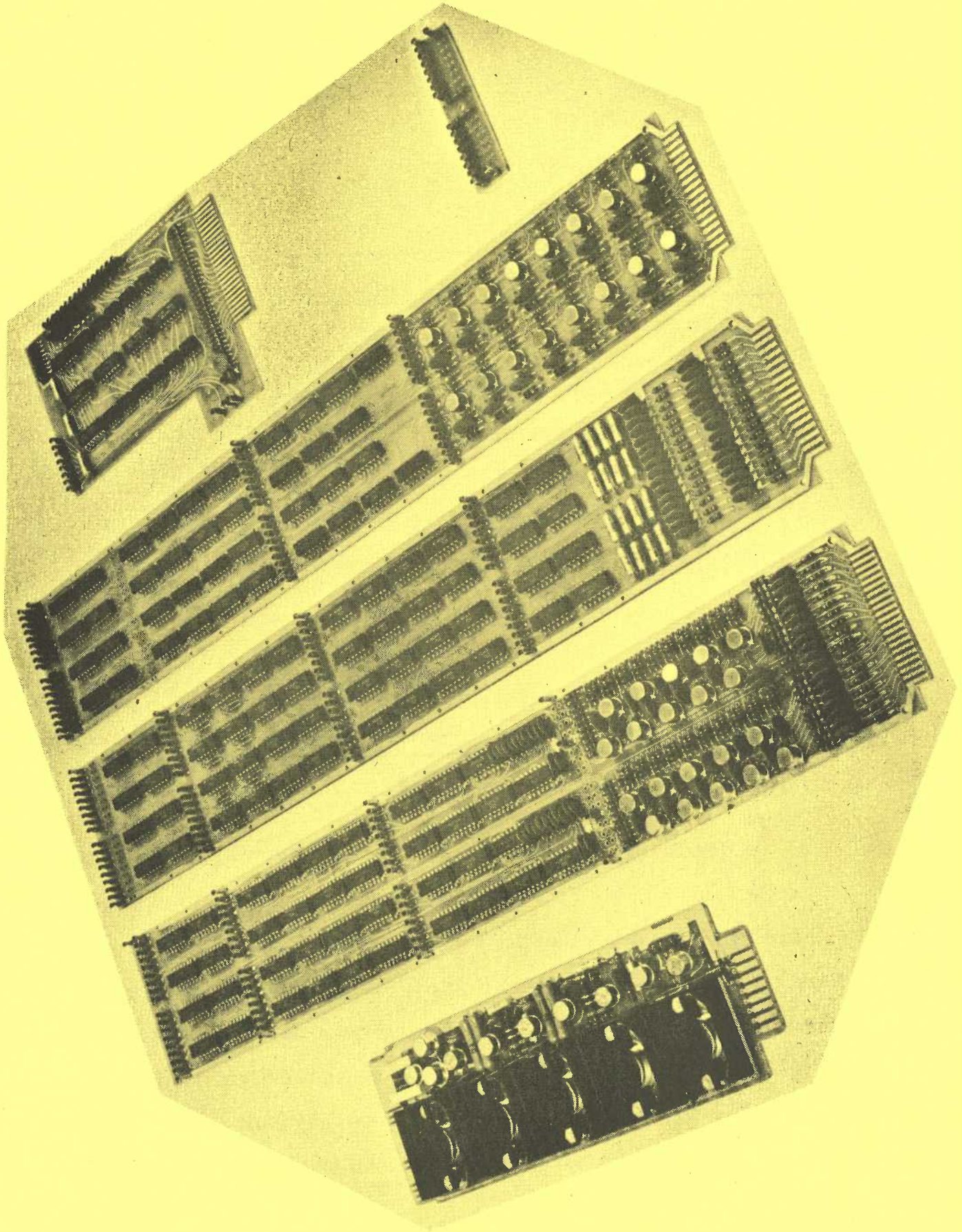

ADDRESS BLOCKS
FUNCTIONAL MODULES
MFM
CPU
I/O SECTION
1
6
11
16
A
ADR 1
2
BYTE 1
BYTE 2
B
3
4
BYTE 1
BYTE 2
C
5
6
BYTE 1
BYTE 2
D
7
8
BYTE 1
BYTE 2

ELECTRICAL SPECIFICATIONS:

NOISE IMMUNITY	1 Volt
INTERNAL LOGIC	TTL and TTL/MSI
POWER REQUIREMENTS	+5 VDC @ 4.5 Amps +15 VDC @ 100ma.

PHYSICAL CHARACTERISTICS:

OPERATING TEMPERATURE	0° to +70° C
MIN. MOUNTING CENTERS	1.1 INCHES
BOARD DIMENSIONS	20.0 X 12.5 INCHES
CONNECTORS	3- 50 PIN .125" CENTERS
BOARD MATERIAL	G-10 GLASS EPOXY
STORAGE TEMPERATURE	-55° to +85° C



DIGITAL INPUT MODULE

FEATURES:

16 INPUT CHANNELS PER MODULE

INPUT SIGNAL BUFFERING

2 INPUT SPEEDS

HIGH NOISE IMMUNITY

ALL CERAMIC INTEGRATED CIRCUITRY

GENERAL DESCRIPTION:

The Digital Input Module is designed to provide interface for 16 input signals to the host processor. Each input channel has two inputs: (1) Input A provides for a contact closure to system common that has a 4 Millisecond delay before output to remove contact bounce, and (2) Input B provides for a semiconductor driver to system common with line filtering for high speed inputs. An input channel test and inhibit control is provided for system control and maintentance. A display output is provided with a test and inhibit control to drive a display to indicate input status for system maintenance.

ELECTRICAL SPECIFICATIONS:

INPUT CHANNELS	16
INPUT VOLTAGE	+15 V.D.C.
INPUT LOADING	15-30 MA.
A INPUT DELAY ON	4 Milliseconds
B INPUT DELAY	28 Microseconds
REGISTER OUTPUT	DTL or TTL
POWER REQUIREMENTS	+15 V.D.C. @ 3.6 Amp Max.
	+5 V.D.C. @ 500 MA. Max.

PHYSICAL CHARACTERISTICS:

OPERATING TEMPERATURE	0° to +70° C
MIN. MOUNTING CENTERS	1.1 INCHES
BOARD DIMENSIONS	3.0 X 17.7 INCHES
CONNECTOR	36 PIN .125" CENTER
BOARD MATERIAL	G-10 GLASS EPOXY
STORAGE TEMPERATURE	-55° to +85° C

DIGITAL OUTPUT MODULE

FEATURES:

16 OUTPUT CHANNELS PER MODULE

CURRENT LIMITING OUTPUTS

HIGH NOISE IMMUNITY

CERAMIC INTEGRATED CIRCUITRY

GENERAL DESCRIPTION:

The Digital Output Module is designed to provide interface output from the host processor into high noise immunity line driver outputs. The line driver output is current limiting to protect against short circuits. The rise and fall times have been conditioned to permit the line driver to drive lines of up to 2000 feet in length. An output channel test and inhibit control is provided for system control and maintenance. A display output is provided with a test and inhibit control to drive a display to indicate output status for system maintenance.

ELECTRICAL SPECIFICATIONS:

OUTPUT CHANNELS	16
OUTPUT VOLTAGE	+15 V.D.C.
OUTPUT CURRENT	60-100 MA. MAX.
REGISTER INPUT	DTL or TTL
POWER REQUIREMENTS	+15 V.D.C. @ 5.6 Amps

PHYSICAL CHARACTERISTICS:

OPERATING TEMPERATURE	0° to +70° C
MIN. MOUNTING CENTERS	1.1 INCHES
BOARD DIMENSIONS	3.0 X 17.7 INCHES
CONNECTOR	36 PIN .125" CENTER
BOARD MATERIAL	G-10 GLASS EPOXY
STORAGE TEMPERATURE	-55° to +85° C

ANALOG INPUT MODULE

FEATURES:

16 INPUT CHANNELS PER MODULE
FAST SETTLING TIME
HIGH SPEED
SHORT CIRCUIT PROTECTION
HIGH RESOLUTION
HIGH INPUT IMPEDANCE
HIGH ACCURACY
LOW OUTPUT RESISTANCE
STABLE

RUGGED CONSTRUCTION

GENERAL DESCRIPTION:

The Analog Input Module is a high speed, high accuracy module utilizing state of the art integrated, MSI, and hybrid circuits. The analog input range is unipolar 0 to +10 V. and the output is 12 bit straight binary. Each analog input contains an A.C. termination to ground for terminating long D.C. transmission lines.

The Star System Analog Input Module contains a 16 channel multiplexer composed of four one-of four multiplexers. Each of the four 4 channel multiplexers is a high speed, high performance unit that is complete with 4 MOS-FET switches, drivers and decoding for selecting one of 4 analog inputs. The multiplexer output is buffered by a high performance voltage follower which protects the FET switches from shorts on the output. The input range is 0 to +10V full scale with a transfer accuracy of $\pm$0.05% and the output is capable of driving an input resistance as low as 2K ohms. The Control inputs are TTL/DTL compatible.

The 16 channel multiplex sequence rate is 100 KHZ and the A-D conversion rate is 50KHZ. This module can operate in either of two modes: under processor control via its digital interface or in a maintenace mode whereby the unit will cycle at a one second rate to facilitate system trouble shooting or maintenance. This allows any analog input to be enabled and converted to the display under manual control.

ELECTRICAL SPECIFICATIONS:

ANALOG CHANNELS	16
ANALOG INPUT VOLTAGE RANGE	0 to +10V FS
INPUT OVERVOLTAGE RANGE	± 15Volts Max.
INPUT IMPEDANCE	10^9 OHM MIN.
ACCURACY	± 0.05% FS
RESOLUTION	12 BINARY BITS
STABLE	± 0.05% /° C
LONG TERM STABILITY	± 0.05% / YEAR
TEMPERATURE COEFFICIENT	± 10PPM/° C of FFS
SEQUENCE RATE	100 KHZ MAX.
SETTLING TIME	5us to ± 0.01% FS
INPUT POWER REQUIREMENTS	+15VDC @ 1 Amp Max. -15VDC @ 350 MA. Max. +5 VDC @ 500 MA. Max.
CONVERSION TIME	50 KHZ MAX.

PHYSICAL CHARACTERISTICS:

OPERATING TEMPERATURE	0° to +70° C
MIN. MOUNTING CENTERS	1.1 INCHES
BOARD DIMENSIONS	3.0 X 17.7 INCHES
CONNECTOR	44 PIN .100 CENTER
BOARD MATERIAL	G-10 GLASS EPOXY
STORAGE TEMPERATURE	-55° to +85° C

ANALOG OUTPUT MODULE

FEATURES:

16 OUTPUT CHANNELS PER MODULE

FAST OUTPUT SWING 12 BIT RESOLUTION

UNIPOLAR/BIPOLAR

RUGGED CONSTRUCTION

GENERAL DESCRIPTION:

The Analog Output Module (AOM) is a high speed, high accuracy module. Each module contains 16 Sample and Hold circuits complete with buffers, registers, and D-A converters. Each output is straight binary and the full scale output can be either unipolar (0 to +10V. @ SMA) or (± 5V @ ± 5MA) by means of external pin programming. Output settling time is 5 uS to ± 0.05% of full scale.

ELECTRICAL SPECIFICATIONS:

OUTPUT VOLTAGE SWING	0 to +10 Volts F.S. ± 5 Volts F.S.
OUTPUT CURRENT	± 5 MA. MAX.
LINEARITY	± 1 LSB
OUTPUT IMPEDANCE	100 MILLIOHMS
OUTPUT SLEWING RATE	10V/USEC
SETTLING TIME	5USEC. to ± 0.05% F.S.
ABSOLUTE ACCURACY	± 0.025% of F.S.
RESOLUTION	12 BINARY BITS
TEMPERATURE COEFFICIENT	± 30 PPM/°C
POWER REQUIREMENTS	+15VDC @ 1 Amp Max. -15VDC @ 350 MA. Max. +5 VDC @ 500 MA. Max.

PHYSICAL CHARACTERISTICS:

OPERATING TEMPERATURE	0° to +70°C
MIN. MOUNTING CENTERS	1.1 INCHES
BOARD DIMENSIONS	3.0 X 17.7 INCHES
CONNECTOR	44 PIN .100 CENTER
BOARD MATERIAL	G-10 GLASS EPOXY
STORAGE TEMPERATURE	-55° to +85° C

SYNCHRONOUS MODEM CONTROLLER

FEATURES:

- FULL OR HALF DUPLEX SERVICE
- AUTOMATIC SYNCHRONOUS DETECTION
- STRAPABLE SYNCHRONOUS CHARACTER
- RESYNCHRONIZE FUNCTION
- PROGRAMMED DATA TRANSFERS (IN AND OUT)
- INTERNAL OR EXTERNAL I/O BUSS CONTROL
- CONTROL BY SOFTWARE, FIRMWARE, OR BOTH
- OPTIONAL AUTOMATIC CALLING UNIT AND/OR ANSWERING

GENERAL DESCRIPTION:

The Synchronous Modem Controller (SMC) enables the computer to transmit serial data over communications lines via a synchronous modem. Data rates up to 9600 baud are available for point to point, multipoint, or switched network. All control functions and interface levels between the SMC and the modem conform to EIA RS 232-B/C standards. Up to 50 foot of cable attachment is provided with the SMC.

ELECTRICAL SPECIFICATIONS:

INPUT VOLTAGE	Bipolar ±25VDC Max. with respect to ground
INPUT IMPEDANCE	3K Min., 7K Max.
OUTPUT VOLTAGE	Bipolar ±8VDC MIN.
OUTPUT CURRENT	Source 3 ma. Sink 15 ma.
RISETIME	2uS Max.
POWER REQUIREMENTS	+12VDC @ 225 ma. -12VDC @ 100 ma. +5 VDC @ 1.4 amps

PHYSICAL CHARACTERISTICS:

OPERATING TEMPERATURE	0° to +70° C
MIN. MOUNTING CENTERS	1.1 INCHES
BOARD DIMENSIONS	3.0 X 17.7 INCHES
CONNECTOR	36 PIN .125 " CENTER and Cinch DP25P or equivalent
BOARD MATERIAL	G-10 GLASS EPOXY
STORAGE TEMPERATURE	-55° to +85° C
CABLE ATTACHMENT	Up to 50 feet specified at site planning

STAR SYSTEM VOLTAGE REGULATOR

GENERAL DESCRIPTION:

The Star System Voltage Regulator is designed to furnish a very stable positive and negative 12-15 volts and a positive 5 volts to any Star System CPU Memory or Multifunctional Module.

The DC input to the regulators is +24 VDC ± 4V for the +12 +15 V.D.C. (including ripple). The +12-+15 V outputs are current limited to 6.0 amps at +15V and the current folds back to approximately .7 amps with the output shorted to ground. Over-voltage protection is provided by a crowbar circuit which turns off the main input supply.

The +12,+15V and -12,-15 V regulators track together and are adjusted by a single control. An adjustment is also provided for the +5V regulator.

Decoupling diodes are provided on the unregulated inputs to protect the regulators from accidental polarity reversals or shorts on the inputs. Diodes are also provided to protect the regulators from polarity reversals accidentally applied to the regulator outputs.

ELECTRICAL SPECIFICATIONS:

INPUT VOLTAGE	+24VDC ±4V including ripple -24VDC ±4V including ripple +12VDC ±4 V including ripple
OUTPUT VOLTAGE/CURRENT	+12, +15 VDC @ 6.0 Amps Max. -12, -15VDC @ 2.0 Amps Max. +5 VDC @ 6.0 Amps Max.
OUTPUT CURRENT LIMIT ±15V	6.0 Amps @ ±15V out 0.7 Amps @ 0V out
OUTPUT CURRENT LIMIT ± 12, 15V	6.0 Amps @ +5V out 0.7 Amps @ 0V out
LOAD REGULATION ± 12, 15V	±0.3 %
LOAD REGULATION ±5 V	±0.3%
LINE REGULATION	±0.05%
RIPPLE REJECTION	0.5 mv/V
TEMPERATURE STABILITY	±0.005%/ C
LONG TERM STABILITY	±0.1%
STANDBY CURRENT DRAIN	+24V - 35ma -24V - 10ma +12V - 35ma

PHYSICAL CHARACTERISTICS:

OPERATING TEMPERATURE RANGE	0 to +70° C
STORAGE TEMPERATURE RANGE	-55° to +85° C
RELATIVE HUMIDITY	Up to 95% non-condensing
BOARD SIZE	8.5 X 2.75 INCHES
CONTACTS	Card edge, 10 position 20 gold-plated contacts, 0.156 centers & 25-50 gold-plated contacts, 0.100 centers

Star System II Control Process Unit

-Hardware Brief-

The Star System II Control Process Unit (CPU) is a microprogrammable digital computer with broad application capabilities and excellent performance at a practical price. It has a control section which is in itself a programmable computer incorporating a control memory and an organized set of microcommands. These microcommands generate the control and timing signals required to perform all control operations and data manipulations in the machine. Command sequences which for microprograms are stored in read only storage. Thus, this CPU can be programmed to emulate instructions of general or special purpose computers or to perform specific applications.

This CPU incorporates a 1.0 microsecond core memory cycle time and a 200 nanosecond command execution time. This speed permits rapid emulation of macro instructions and can be used to minimize interface hardware by applying the speed of the machine to interface functions.

The modular electrical and mechanical design of this CPU results in the flexibility needed to apply it to a wide range of dedicated process control applications. The modular design of the core memory read only storage, processor options, and input/output elements permits expansion of the system as required.

The Star System II CPU uses TTL monolithic integrated circuits including a large number of the medium scale integration type for savings in parts and assembly time. The use of a read only storage for control further reduces the number of circuits that might otherwise be required to provide the same functional capability. Packaging and powering of this CPU has been designed for small "micro" systems resulting in a savings in system cost.

Star System II CPU Features

Memory addressing to 65K

4K or 8K memory modules

1.0 microsecond memory speed (full cycle)

8, 9, or 10 bit memory bytes for efficient character handling extra bits for memory parity and special applications

Direct memory access (DMA) option

30 general purpose eight-bit file registers

Up to 32,768 words of read only memory

200 nanosecond microcommand execution time

Real-time clock (optional)

Memory protect (optional)

Power-fail option for automatic shutdown in the event of a power failure, and automatic startup when power returns

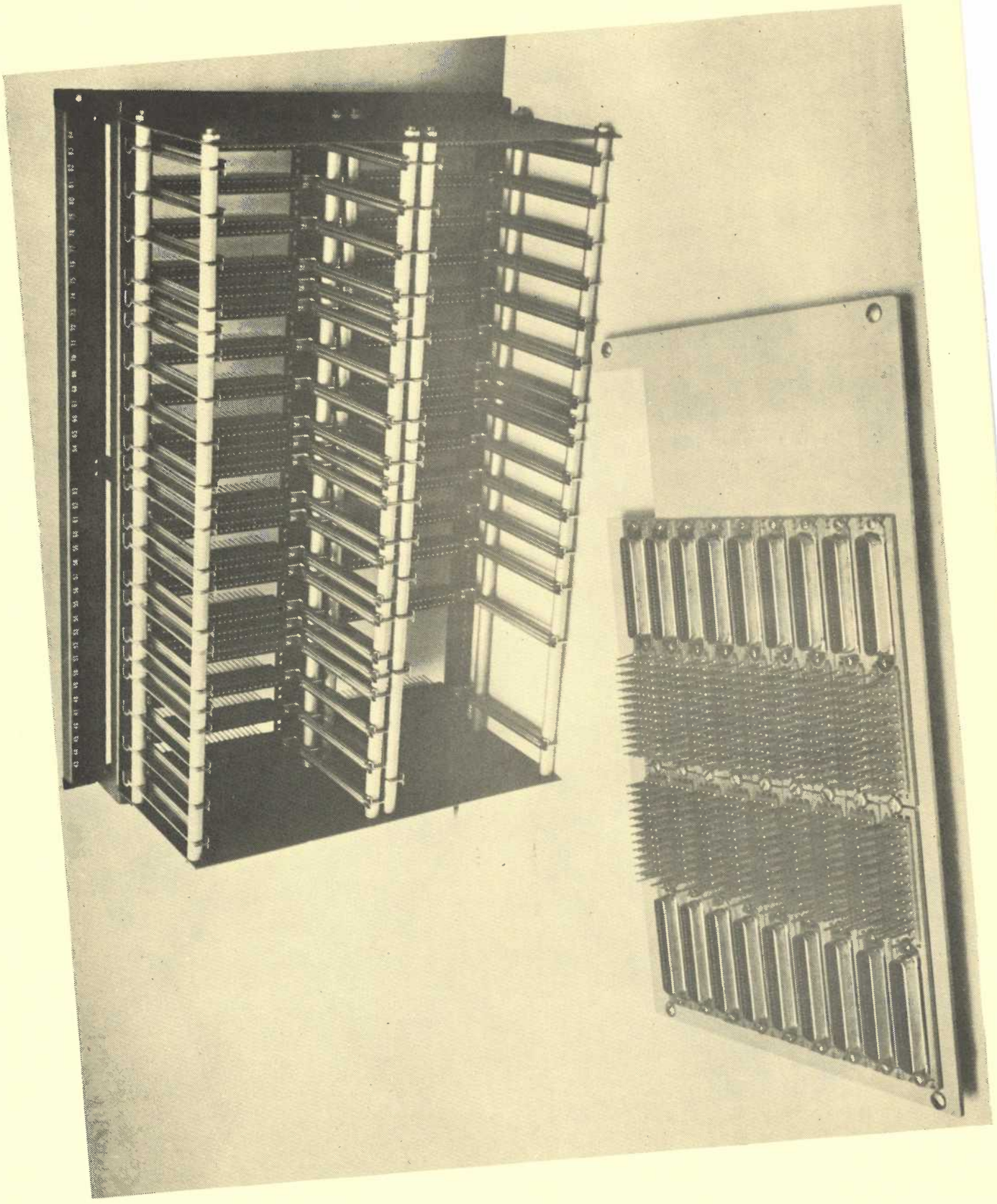
Seven I/O transfer modes

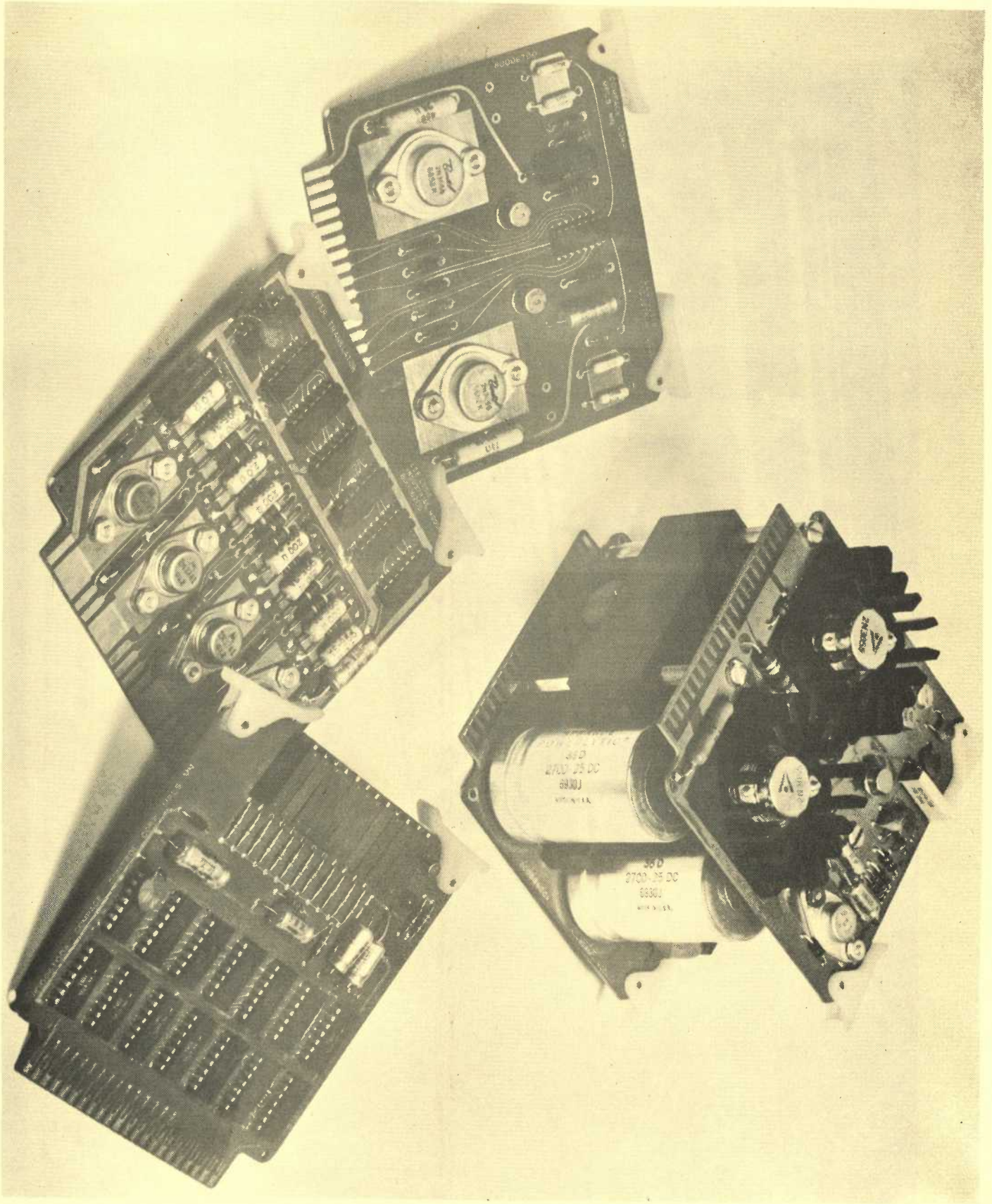
15 basic commands

TTL integrated circuitry

Operating temperature range 0 degrees C to 50 degrees C

Power: 115/230 VAC, 50-60 cycle





NEW ADVANTAGES IN SYSTEM CONTROL

The Process Engineer's ability using PCL to understand and write the software for his system also gives him several very valuable and cost-saving capabilities once his control system is fully operational. If a more efficient machine or system operating procedure is discovered, for instance, the Process Engineer can change the control equations of his system to take advantage of the new development. If system management can be greatly aided by certain types of information about system operation, the Process Engineer can often retrieve that data from his system through a modification of his programs. And finally, if some system malfunction should occur, the Process Engineer, through adept programming, can quickly locate and in some cases by-pass the troubled area until repairs can be effected.

PROVEN COMPATIBILITY AND ADAPTABILITY

COMSTAR's Process Control Language in conjunction with Star System hardware offers a highly adaptable control package which can be designed around a user's needs and which can be made compatible with the user's existing control equipment if necessary. Thus, system expansion can be accomplished at minimum cost with maximum results in system performance.

PCL allows the Process Engineer to smoothly integrate the new control equations of a Star System minicomputer with the old control patterns of system operation. Whole sets of industrial control panels and solid state module racks can be brought under the direction of one minicomputer through PCL and the powerful interface capability of Star System hardware.

PROVEN COMPATIBILITY AND ADAPTABILITY (continued)

If even further system expansion is desired, the Star System minicomputers and PCL are compatible with larger computer systems such as the IBM 360. This proven compatibility and adaptability makes PCL an integral and valuable part of COMSTAR's package approach to control process design.

I. AN INTRODUCTION TO PCL

COMSTAR Corporation's new Process Control Language is a significant breakthrough in the field of microprogramming for industrial and material systems applications. PCL eliminates a major stumbling block in the minicomputer management of a control process by uniting the functions of Process Engineer and System Programmer. COMSTAR's PCL permits this efficient and cost-saving move because it is a computer language which an engineer can learn quickly and which is tailored to his programming needs.

PCL is easily mastered even by someone without previous programming experience because its language format closely resembles standard English and its symbols are drawn from traditional relay logic. All instructions in PCL are specially designed for the solution of problems in system operation.

Since the Process Engineer can do the programming the purchaser of a COMSTAR system need only pay an initial one-time only software charge. PCL thus helps avoid expensive call-backs and delays for programming help.

No minicomputer is better than the array of instructions available to its controller. COMSTAR's PCL boasts a powerful control capability on the basis of only 34 control instructions. Using only this small number of commands, the Process Engineer can write equations to govern the operation of his entire process control system.

II. BACKGROUND ON PCL PRINCIPLES

A. The Binary Concept

The control commands of PCL are based upon a consideration of two-state type decisions. There are a large number of devices with only two states or possible conditions. For example, a light switch has only two states: it can be on or off. Similarly, a doorbell button can be either pressed or released, causing a bell to be on or off. A production machine can only be ready for operation or not ready. Decisions, in such circumstances, are often based upon a number of YES or NO type conditions. Logical decisions of this type can be efficiently translated into electronic circuitry through the medium of electrical gates.

B. Electrical Gates

The electrical gates of Star System minicomputers permit a Process Control Engineer to write control decisions into a general program to direct the operation of his system. By using gates and other devices, the Engineer simply translates the control logic of his drawing board into the programmed circuitry of his minicomputer. The five general types of gates used in the Star System minicomputers are described below.

1. OR Gate: the result or output of an OR gate is dependent upon the inputs or conditions examined by the OR gate according to the

following table (YES = HI = TRUE):

INPUTS		OUTPUT
A	B	C
NO	NO	NO
NO	YES	YES
YES	NO	YES
YES	YES	YES

Standard OR Symbol

2. AND Gate: the result or output of an AND gate is dependent upon the inputs or conditions examined by the AND gate according to the following table:

INPUT		OUTPUT
A	B	C
NO	NO	NO
NO	YES	NO
YES	NO	NO
YES	YES	YES

Standard AND Symbol

3. NAND gate: the result or output of a NAND gate is dependent upon the inputs or conditions examined by the NAND gate according to the following table:

INPUT		OUTPUT
A	B	C
NO	NO	YES
NO	YES	YES
YES	NO	YES
YES	YES	NO

Standard NAND Symbol

4. Inverter gate: the result or output of an Inverter gate is the direct inverse of the input condition according to the following table:

INPUT	OUTPUT
A	B
YES	NO
NO	YES

Standard Inverter Symbol

5. Exclusive Or gate: the result or output of an Exclusive Or gate is dependent upon the inputs or conditions examined by the Exclusive Or gate according to the following table:

INPUTS		OUTPUT
A	B	C
YES	YES	NO
NO	YES	YES
YES	NO	YES
NO	NO	NO

Standard Exclusive Or Symbol

Thus, these five gates are key parts of the system which makes PCL possible. A second major component is memory which is important in programming and created by the use of devices known as flip-flops.

C. Flip-Flops

The logic devices discussed to this point have all required a continuous input level to operate. Once this input signal was removed, the device would not remember its previous input condition. In addition to gates, a computer requires devices that will retain their condition after an input has been removed

In the Star System minicomputers, one device which has a memory is called a flip-flop: an electronic element which remembers the last instruction it received. In many ways, it is similar to a light switch. If a flip-flop receives an instruction to go to the " 1 " (or YES) condition it does so and stays there until instructed to go to the "0" condition (and vice versa).

All flip-flops have a 1 and 0 output. If the 1 output is HI, it indicates that the flip-flop is in the "1" condition. If the 0 output is HI, the flip-flop is in the "0" condition. The table below shows the two possible output conditions for a flip-flop, and the flip-flop state.

OUTPUTS		FLIP-FLOP STATE
1	0	
HI	LO	"1"
LO	HI	"0"

III. PCL INSTRUCTIONS

These next few pages will define and explain the array of instructions available with the Star System Process Control Language. Each definition will include a description of the necessary addresses associated with the given command. In most cases the addresses are 16 bits in length and refer to the computer's Read/Write Memory. The contents of this address is the value used by the instruction. The instruction's symbol in machine language - a number in the computer code - is also shown along with an example to facilitate understanding the language.

PCL instructions fall into seven identifiable categories:

A. Logical
B. Arithmetic
C. Input/Output
D. Data Control
E. Data Compare
F. Branch
G. Message Output

On the following pages, the instructions in each category will be listed, defined, and explained.

A. Logical Instructions

The Logical group of PCL instructions are designed to assist the Process Engineer in writing equations which decide, under certain conditions, what computer control responses should be activated. Logical instructions do not refer to addresses in the computer like other PCL instructions do. Instead, they refer to computer codes (INLy, OUTy, XINy, MEMz) which represent Input/Output lines or memory registers. These special codes will be defined in part # 9 of this section. For the moment, they will be symbolized by the phrase "condition 1".

1. INSTRUCTION: IF condition 1
   EXPLANATION: Causes execution of a statement if condition 1 is true.
   EXAMPLE: If conveyor lines are full, go to the beginning of the program.
   SAMPLE EQUATION: IF INL5 GOTO 1000
   COMPUTER CODE NUMBER: 20

2. INSTRUCTION: IF-NOT condition 1

EXPLANATION: Identical to IF, exept the value of condition 1 is complimented.

EXAMPLE: If all the sub-conveyors are not empty then stop the main conveyor motor.

SAMPLE EQUATION: IF-NOT MEM 10 CLEAR OUT 6.

COMPUTER CODE NUMBER: 21

3. INSTRUCTION: AND condition 1

EXPLANATION: The result of the previous instruction and the value called by condition 1 are AND'ed together.

EXAMPLE: If machines # 5 & # 7 are busy, then go to the end of the program.

SAMPLE EQUATION: IF INL 5 AND INL 7 GOTO 5000.

COMPUTER CODE NUMBER: 22

4. INSTRUCTION: AND-NOT condition 1

EXPLANATION: The value referred to in condition 1 is complimented and then AND'ed together with the result of the previous instruction.

EXAMPLE: If the conveyor line is not full, and machine #1 is not operational, then display a warning signal by clearing output line 65.

SAMPLE EQUATION: IF-NOT MEM 50 AND-NOT MEM-71 CLEAR OUT 65.

COMPUTER CODE NUMBER: 23

5. INSTRUCTION: OR condition 1

EXPLANATION: The value of condition 1 is OR'ed with the value of the previous instruction.

EXAMPLE: If machine #1 or machine #2 has completed an operational cycle, increment the product counter by one.

SAMPLE EQUATION: IF MEM-50 OR MEM 52 INCTR 1100,

COMPUTER CODE NUMBER: 24

6. INSTRUCTION: OR-NOT condition 1

EXPLANATION: The value of condtiion 1 is complimented and then OR'ed with the value of the previous instruction.

EXAMPLE: If the divertor conveyors are full or machine #1 is not ready return to the beginning of the program.

SAMPLE EQUATION: IF INL 10 OR NOT INL 20 GOTO 1000.

COMPUTER CODE NUMBER: 25

7. INSTRUCTION: THEN condition 1

EXPLANATION: The result of the previous instruction (HI = TRUE) determines whether condition 1 will be acted upon.

EXAMPLE: If the conveyor line is running and machine #1 is ready, then begin the flow of raw material to the conveyor.

SAMPLE EQUATION: IF INL 5 AND MEM 100 THEN OUT 76.

COMPUTER CODE NUMBER: 26

8. INSTRUCTION: THEN-NOT condition 1

EXPLANATION: The result of the previous instruction determines whether the compliment of condition 1 will be acted upon.

EXAMPLE: If warning signal a or b are operative then - stop all conveyors immediately.

SAMPLE EQUATION: IF INL 6 OR INL 8 THEN-NOT OUT 84.

COMPUTER CODE NUMBER: 27

9. The following four computer codes are used in conjunction with Logical instructions for convenience in calling out Input/Output lines and memory registers (programmable flip-flops). The PCL compiler program converts this code to a format useable by the internal machine language of the Star System CPU.

a. INLy (INput Line y)
This code designates a unique input line (y is a decimal number from 1 to 512) to the CPU. Input line 200, for example, might be a line from a sensor scanning a certain sub-conveyor.

b. OUTy (OUTput Line y)
This code designates a unique output line (y is a decimal number from 1 to 512) from the CPU. Output line 500, for example, might activate a motor which would start a machine.

c. XINy

This code specifies a unique input "line" that has had an Exclusive OR performed between the most recent and previous input. When this "line" changes state it signifies that actual input line has changed state. For example, a sensor observes that a machine which has been busy with an operation suddenly finishes the product and is ready for another input of raw material.

d. MEM z

This code specifies a unique programmable flip-flop in memory (z is a decimal number ranging from 1 to 1024) that can be set or cleared by equation control. This code is useful in "holding" a condition of an input line that is of a very short duration. For example, if a sensor shows a production machine is temporarily overheating, this code would permit the Process Engineer to keep an ALERT light on constantly rather than just an occasional flicker.

B. Arithmetic Instructions

1. INSTRUCTION: ADD address 1, address 2, address 3

EXPLANATION: The contents of memory locations as pointed to by addresses 1 & 2, are algebraically added with the result stored in memory as indicated by address 3. The result (i.e. the sum) can range in value from + $32,767_{10}$.

SAMPLE EQUATION: ADD 1200, 1564, 1200

COMPUTER CODE NUMBER: 08

2. INSTRUCTION: SUB address 1, address 2, address 3

EXPLANATION: Performs the subtract function by subtracting the contents of memory as pointed to by address 2 from the contents of memory as indicated by address 1. The result is stored in memory as indicated by address 3. The range of the difference is + $32,768_{10}$.

SAMPLE EQUATION: SUB 1206, 1500, 13AC

COMPUTER CODE NUMBER: 09

3. INSTRUCTION: ABSDIF address 1, address 2, address 3

EXPLANATION: Identical to SUB except the result is always a positive number.

SAMPLE EQUATION: ABSDIF 708 712 15AE

COMPUTER CODE NUMBER: 0A

4. INSTRUCTION: MULT address 1, address 2, address 3

EXPLANATION: The contents of addresses 1 & 2 are multiplied together with the result (i.e. product) stored in memory as indicated by address 3. The product can range in value from + $32{,}767_{10}$.

SAMPLE EQUATION: MULT 1448 1450 1678

COMPUTER CODE NUMBER: 0B

5. INSTRUCTION: DIV address 1, address 2, address 3

EXPLANATION: The contents of address 1 are divided by the contents of address 2 with the result (i.e. quotient) stored in memory as indicated by address 3.

SAMPLE EQUATION: DIV 1668 16C0 1668

COMPUTER CODE NUMBER: 0C

C. Input/Output Instructions

1. INSTRUCTION: ESCD

EXPLANATION: This instruction causes all digital I/O to be performed and creates the Exclusive OR buffer. The ExOR buffer is created by doing an Exclusive OR of the new input with the previous input data. The result is a 1 only if the input line has changed state. The ExOR result is zero if no change in state has occurred. NOTE: The ESCD instruction must be used only once per process cycle, otherwise equations will not correctly sense changes to input lines.

SAMPLE EQUATION: ESCD

COMPUTER CODE NUMBER: 19

2. INSTRUCTION: RDALOG address 1

EXPLANATION: Address 1 is a decimal number from 1-128 specifying a unique Analog input address. NOTE: Care must be taken in using this instruction due to physical limitations of the hardware. In order to insure that the required data is input, from six to eight equations should separate the RDALOG instruction from any instruction which utilizes the data stored in the RDALOG address 1 or from any other RDALOG instruction. If this is not done, the analog data will be improperly read by the computer.

SAMPLE EQUATION: RDALOG 60 (6-8 equations = 150 usecs) IF 500 EQ 1600 THEN OUT 412. Where 500 contains the analog value from the RDALOG input equation.

COMPUTER CODE NUMBER: 1A

D. Data Control Instructions

1. INSTRUCTION: MOV1 address 1, address 2
   EXPLANATION: The contents of address 1 (8 bits) are moved to address 2.
   SAMPLE EQUATION: MOV1 736 2154
   COMPUTER CODE NUMBER: 01

2. INSTRUCTION: MOV2 address 1, address 2
   EXPLANATION: Identical to MOV1 except the value moved is 16 bits in length.
   SAMPLE EQUATION: MOV2 738 2156
   COMPUTER CODE NUMBER: 02

3. INSTRUCTION: MOV3 address 1, address 2
   EXPLANATION: Identical to MOV1 except the value moved is 24 bits in length.
   SAMPLE EQUATION: MOV3 738 2160

4. INSTRUCTION: MOV4 address 1, address 2
   EXPLANATION: Identical to MOV1 except the value moved is 32 bits in length.
   SAMPLE EQUATION: MOV4 740 2164
   COMPUTER CODE NUMBER: 04

5. INSTRUCTION: CLEAR line 1

EXPLANATION: This instruction caused the designated line (1 bit in a register or output buffer word) to be set to 0.

SAMPLE EQUATIONS:
```
CLEAR MEM 100
IF XIN 1 CLEAR OUT 158
```

COMPUTER CODE NUMBER: 12

6. INSTRUCTION: SHIFT address 1

EXPLANATION: This address points to a 16 bit shift register which is shifted right one bit position. If a bit is shifted off the right end, a true condition exists and an internal indicator is set for the following instructions.

SAMPLE EQUATIONS:
```
SHIFT 1436 THEN OUT 400
```

COMPUTER CODE NUMBER: 13

7. INSTRUCTION: SET SFT address 1, address 2

EXPLANATION: This instruction denotes which particular bit defined by the literal value from 1-16 in address 2 is set in the designated shift register pointed to by address 1. In the example below, bit 9 of the shift register pointed to by 1436 is set to a one.

SAMPLE EQUATION:
```
IF XIN 106 SETSFT 1436 .9.
```

COMPUTER CODE NUMBER: 14

8. INSTRUCTION: SET line 1

EXPLANATION: This instruction causes the designated line (1 bit in a register or output buffer word) to be set to 1.

SAMPLE EQUATION: SET MEM 56

COMPUTER CODE NUMBER: 11

9. INSTRUCTION: INCTR address 1

EXPLANATION: This instruction causes a 32 bit counter, specified as a Hexidecimal Memory address by address 1 to be incremented by 1.

SAMPLE EQUATION: INCTR 1200

COMPUTER CODE NUMBER: OD

10. INSTRUCTION: DECTR address 1

EXPLANATION: This instruction causes a 32 bit counter, specified as a Hexidecimal Memory address by address 1 to be decremented by 1.

SAMPLE EQUATION: DECTR 1400

COMPUTER CODE NUMBER: OE

E. Data Compare Instructions

1. INSTRUCTION: EQ address 1

   EXPLANATION: This instruction compares a value designated by the address preceeding EQ with the 16 bit value pointed to by address 1. If the result is true, the statement is interpreted as true. In the example below, if the values in 750 and 79A are equal, MEM 506 would be cleared, otherwise it would remain in its former state.

   SAMPLE EQUATION: IF 750 EQ 79A CLEAR MEM 506

   COMPUTER CODE NUMBER: 05

2. INSTRUCTION: GT address 1

   EXPLANATION: Similar to EQ except a Greater-Than condition is checked for.

   SAMPLE EQUATION: IF 1200 GT 76A THEN OUT 76

   COMPUTER CODE NUMBER: 06

3. INSTRUCTION: LT address 1

   EXPLANATION: Similar to EQ except the Less-Than condition is checked for.

   SAMPLE EQUATION: IF 1200 LT 76C THEN OUT 78.

   COMPUTER CODE NUMBER: 07

F. Branch Instruction

1. INSTRUCTION: GO TO address 1

EXPLANATION: This instruction causes control to be transferred to the location pointed to by address 1. The transfer can be conditional (i.e. depending on a particular state of a line or result of a data compare) or the transfer can be unconditional. If address 1 is of the form SN XXXX, then it refers to the statement number XXXX within the program.

SAMPLE EQUATIONS:

a. Conditional Transfers:

IF XIN 100 GO TO 2050

IF XIN 100 GO TO SN100

IF 1200 GT 1300 GO TO 2254

b. Unconditional Transfers

GO TO 2000

GO TO SN500

COMPUTER CODE NUMBER: 15

G. Message Output Instructions

1. INSTRUCTION: PRINTM address 1

EXPLANATION: Address 1 points to a message residing in core memory that can be outputed on the Star System Printer when this instruction is used. The message as stored in memory has a special format that must be adhered to for correct output:
Message CR LF ETB
Where CR is a carriage return, LF is a line feed and ETB a speical control character. Additionally all characters must be in ASCII format.

SAMPLE EQUATIONS: PRINTM 1000

COMPUTER CODE NUMBER: 16

2. INSTRUCTION: PRINT 1 address 1, address 2

EXPLANATION: Address 1 points to an 8 bit value located in read/write memory. Address 2 is a label of from 1-5 ASCII characters. The PRINT 1 instruction will access the counter designated by address 1, prefix it with a label from address 2, and print it out on the Star System Printer.

SAMPLE EQUATION: PRINT 1 1000 OVEN5

COMPUTER CODE NUMBER: 17

3. INSTRUCTION: PRINT 2 address 1, address 2

EXPLANATION: Identical to PRINT 1 except address 1 points to a 16 bit value located in read/write memory.

SAMPLE EQUATION: PRINT 2 2000 MACH 7

COMPUTER CODE NUMBER: 18

4. INSTRUCTION: PRINT 3 address 1, address 2

EXPLANATION: Identical to PRINT 1 except address 1 points to a 24 bit value located in read/write memory.

SAMPLE EQUATION: PRINT 3 3000 CONV 4

COMPUTER CODE NUMBER: 19

5. INSTRUCTION: PRINT 4 address 1, address 2

EXPLANATION: Identical to PRINT 1 except address 1 points to a 32 bit value located in read/write memory.

SAMPLE EQUATION: PRINT 4 DIVR 9

COMPUTER CODE NUMBER: 1A

WRITING PCL EQUATIONS

PCL instructions by themselves serve no function. When grouped together in equations and programs, however, they become powerful instruments in the control of a system process and the operation of a Star System CPU. Although the specific techniques used to write PCL equations in each application vary widely a general outline of proper operating procedure can be defined.

(1) The first step in this process is a specific and detailed listing of all machine operations and their relationship to input and output devices in the system to be controlled or monitored. The Process Engineer must be careful to list all separate control functions by dividing the operation of machines, for instance, into their smallest parts.

(2) The Engineer should then assign input and output lines to all the appropriate equipment in the control system. Devices such as a photocell sensor may require only one data input line whereas a motor may require two data output lines (one for a motor on signal and another for a motor off signal). It is very important that a logical organization be employed in the distribution and numbering of these I/O lines since this greatly simplifies both system programming and system maintenance.

(3) The third step in this procedure calls for the Process Engineer to list all counting operations and timing operations and assign counters and timers.

(4) The Engineer is now prepared to write equations defining and controlling the operation of the Star System. For each operation defined in step # 1, he should write logic equations using the I/O lines defined in step # 2, and/or the counter/timer assignments made in step # 3.

(5) These written equations should then be grouped in a logical relationship to one another and integrated into the total control system design. For instance, if many different types of machines performing distinct functions are connected in a single line of production the equations for each separate machine should be clustered together and these groups then linked together into the final constellation of control commands which govern the Star System CPU.

Once the Engineer has designed and documented the specific control equations required for his system, he is in a position to estimate fairly accurately the specific hardware requirements for his system. From the number of digital and analog input and output lines in the system and the type and number of peripheral devices needed, he can judge the number and type of Functional Modules, Multifunctional Modules, and Memory Blocks required for control of his system.

AN EXAMPLE OF PCL IN ACTION

-AN AUTOMATIC PACKAGE DIVERTOR SYSTEM-

Step 1 - SYSTEM DEFINITION AND DESCRIPTION

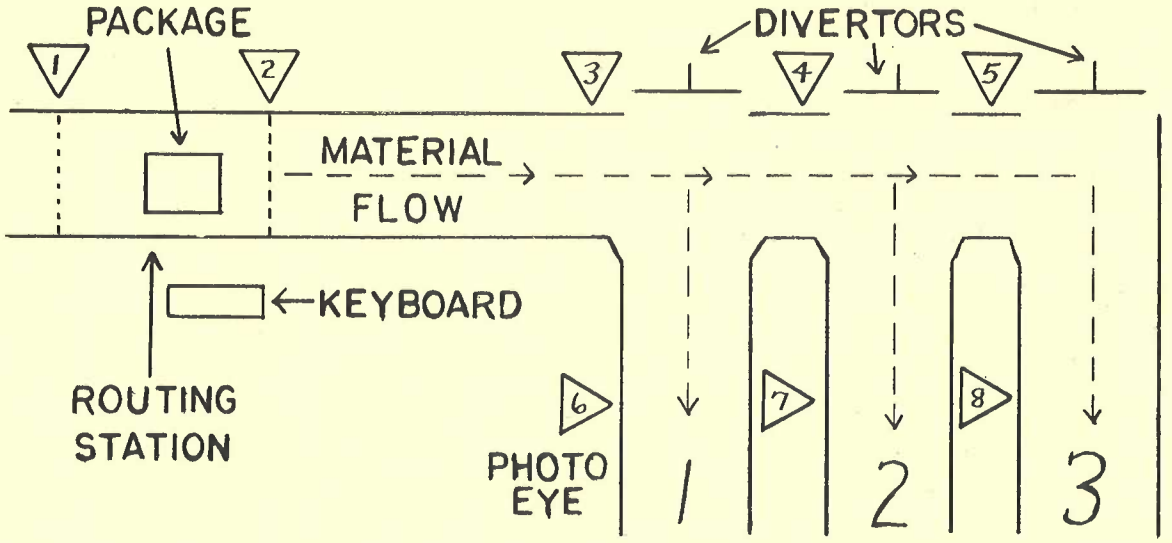
The function of the system is the automation of a package conveyor system such that as each package enters the system it is:

1. Assigned a routing number.
2. Spaced on the conveyor line.
3. Diverted from the main conveyor line to a subline or destination line.

The Automatic Divertor System is made up of powered and gravity feed conveyors, motor switches, sensors, photo eyes, package divertor stations and a routing station. The motor switches and sensors are used to control the starting and stopping of the conveyors on command from the Process Control Computer. The photo eyes detect the presence of packages at specific points along the conveyor lines. The divertors, activated by the computer, physically cause a package to move from the main line onto a subline. The routing station is the point at which an operator looks at a package, determines its destination and keys it into a special keyboard for entry into the computer memory.

PACKAGE FLOW

The following diagram shows an automated system with a routing station, three (3) divertor stations with the associated sublines, and eight (8) photo eyes for package detection.



A package enters the routing station and halts momentarily while the route (subline) number is entered into the computer via a keyboard. When the entry is complete, the package proceeds thru the system with the computer remembering and tracking the package. When a package enters a divertor area and the route number matches the divertor station number the divertor arm is activated and pushes the package onto the subline.

Step 2 - ASSIGNING I/O LINES AND ADDRESSES

The next step in preparing PCL equations for the Automatic Package Divertor System calls for the definition of Input/ Output lines and memory locations.

Program preliminary definitions:

Input lines 1-8	Photo eyes
Output lines 1-3	Package divertors
Output line 4	Stop conveyor line
Output line 5	Start conveyor line
Memory Register 1	=1 when timer reaches x no. of changes
Memory Register 2	Denotes line is stopped

Address Assignments

400	Shift register for divertor 1
402	Shift register for divertor 2
404	Shift register for divertor 3
550	Keyboard input word
511	Constant = 1
512	Constant = 2
513	Constant = 3

Step 3 - ASSIGNING TIMERS AND COUNTERS

Only one timer is needed in the context of this example. Therefore let:

Input line 9	Time base oscillator

Address Assignments

500	Time base multiplier constant
600	Timer counter

These assignments complete the preliminary definition of the required timer.

Step 4 - WRITING THE SAMPLE PROGRAM

In the interest of simplicity certain portions of the sample program have been deleted. For example, stopping the conveyor for routing and checking that packages are in a divertor station have been left out of this sample program. Nevertheless, the following program is sufficient fro an overall idea of PCL use and flexibility.

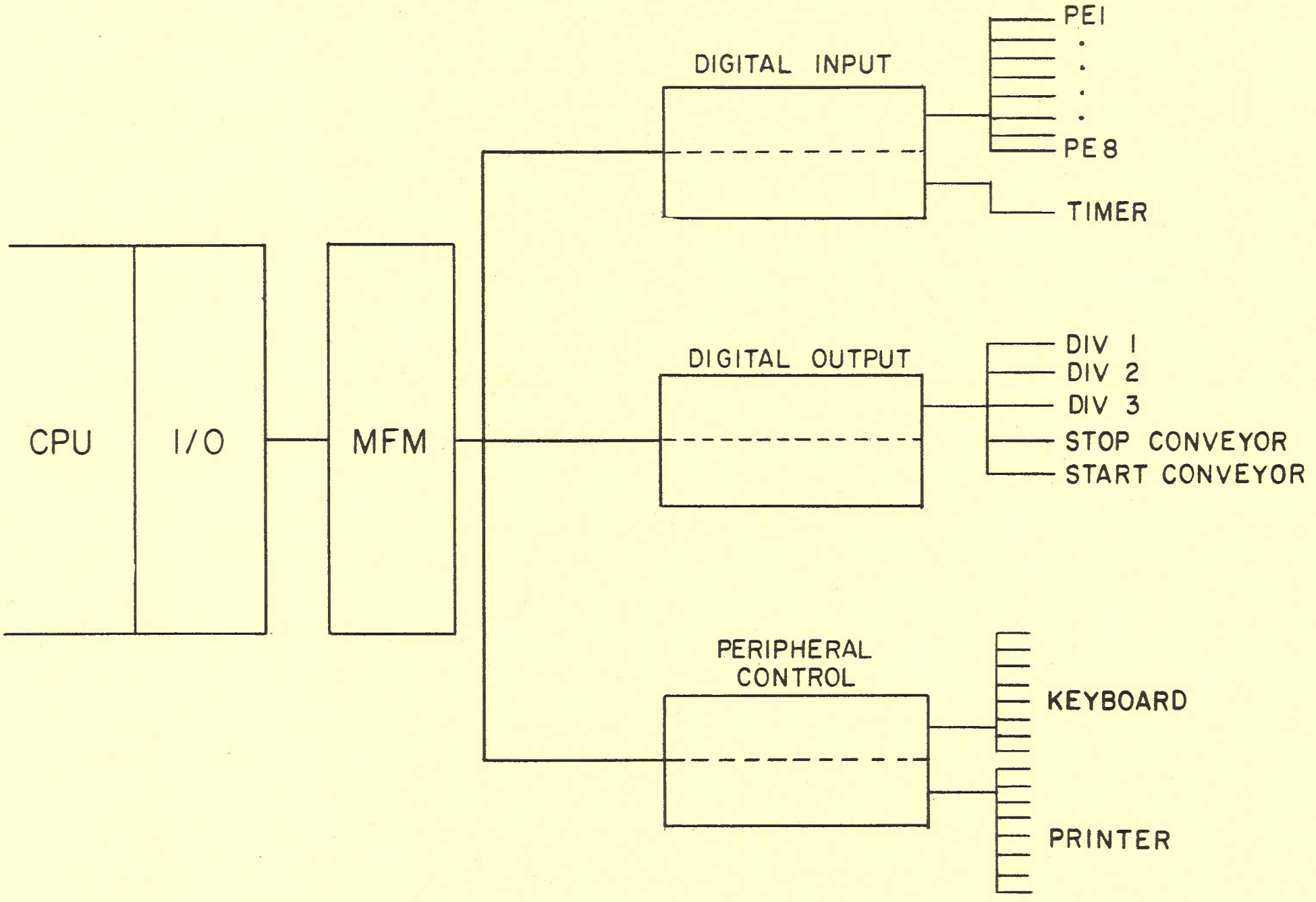
The NOTE statements following each instruction below are for explanatory purposes only and perform no meaningful function.

```
10      ESCD
        NOTE:  This activates all input and output signals
               from the computer.

20      IF INL6 OR INL7 OR INL8 SET MEM 2 THEN OUT 4
        NOTE:  If any sublines are backed-up, stop the conveyor.

30      IF MEM 2 GOTO SN100
        NOTE:  If MEM 2 is set skip the control equations and
               wait until the sublines are all open.

40      IF XIN 9 INC 600
        NOTE:  When the time oscillator changes increment the
               counter.

50      IF 600 EQ 500 SET MEM 1
        NOTE:  If the timer counter equals a preset number,
               then all packages have moved a unit distance
               on the conveyor line.

60      IF MEM 1 SHIFT 400 THEN OUT 1
        NOTE:  If a bit has just been shifted off register 400
               then activate divertor arm 1 because a subline
               # 1 package has just reached its station.
```

```
70      IF MEM 1 SHIFT 404 THEN OUT 3
        NOTE:  If a bit has just been shifted off register 404
               then activate divertor arm 3 because a subline
               # 3 package has just reached its station.

75      IF NOT MEM 1 GOTO 10
        NOTE:  If the MEM 1 register is not set return to the
               beginning and continue to wait until the
               packages have moved a unit distance on the
               conveyor.

80      IF 550 EQ 511 SETSFT 400 2
        NOTE:  If the keyboard input matches the code for
               subline # 1 then set bit 2 in shift register
               400 true (or HI).  Once the conveyor has moved
               all packages two unit distances this bit will
               be shifted off the 400 register and allow
               statement 60 to activate divertor arm 1.

85      IF 550 EQ 512 SETSFT 402 4
        NOTE:  If the keyboard input matches the code for
               subline # 2 then set bit 4 in shift register
               402 true (or HI).  Once the conveyor has moved
               all packages four unit distances this bit will
               be shifted off the 402 register and allow
               statement 65 to activate divertor arm 2.

90      IF 550 EQ 513 SETSFT 404 6
        NOTE:  If the keyboard input matches the code for
               subline # 3 then set bit 6 in shift register
               404 true (or HI).  Once the conveyor has moved
               all packages six unit distances this bit will
               be shifted off the 404 register and allow
               statement 70 to activate divertor arm 3.

93      CLEAR MEM 1
        NOTE:  This clears MEM 1 register in preparation for
               another pause while the conveyor moves all
               packages one unit distance.

95      GOTO SN10
        NOTE:  Go to the beginning of the program and execute
               all the proper control signals.
```

```
100     IF NOT INL 6 AND NOT INL 7 AND NOT INL 8 CLEAR MEM 2
        THEN OUT 5
        NOTE:  When all sublines are clear then clear MEM 2
               and permit the conveyor to run again.

105     GOTO SN10
        NOTE:  Return to the beginning of the program.
```

The Block Diagram on the following page shows how the Process Engineer can visually represent the organization of his control system and in doing so determine its hardware requirements.


CPU
I/O
MFM
DIGITAL INPUT
PE1
PE 8
TIMER
DIGITAL OUTPUT
DIV 1
DIV 2
DIV 3
STOP CONVEYOR
START CONVEYOR
PERIPHERAL CONTROL
KEYBOARD
PRINTER

COMPILING PCL PROGRAMS

The inner workings of the PCL are detailed and require a specific format. The burden of proper formatting and data conversion is handled by the PCL Compiler program. The purpose of this section is to explain the means by which the Process Engineer compiles the set of programs he has written for his control system. Each control program, it has been noted, should govern a separate segment of the control system. Similarly each program should also be compiled separately so that if a program change is required it can be done with a minimum of effort. The basic steps involved in compiling a PCL program are as follows:

(1) Load the Compiler and Edit programs, available from Comstar Corporation on magnetic tape cassettes, into the Star System CPU.

(2) Using the Edit program create a source tape for each unique PCL program. A source tape is a reproduction of the original PCL program on a magnetic tape in a code recognizable to the Compiler program resident in the Star System CPU.

(3) Rewind the source tape on completion of the Edit program. Initiate the Compiler program by command from the Star System keyboard or console. The Compiler program will now read the source tape for the first of two passes.

(4) Upon completion of the first pass the source tape must be rewound. A second magnetic tape recorder must then be loaded with a blank magnetic tape.

(5) The source tape is now read for the second time by the Compiler program. During this second pass the Compiler program will output an object program onto the blank magnetic tape. An object program tape is an ordered translation of the source tape into machine language readable by the Star System CPU. In addition, the Compiler program will output to the Star System Printer a written record of the source tape equations and the associated object tape machine language.

(6) The procedure outlined in steps 3, 4, and 5 can be repeated to compile each separate program.

(7) When the compilation of programs is complete the resulting object tapes can be loaded into the memory of the Star System CPU. This group of object tapes together forms the Program File of the CPU. Before these programs can be executed, however, the Star System Executive Program must be loaded into the CPU. This program interprets the Program File and directs the operation of the Star System CPU. The Compiler and Edit programs cannot coexist in the CPU with the Star System Executive Program. Therefore, when the compilation of programs is complete and the

Star System Executive Program is loaded the Compiler and Edit programs will be overwritten.

(8) Once the Program File is complete and the Executive Program is loaded the Process Engineer is prepared to begin operating the entire process control system.

STAR SYSTEM I PRICING INFORMATION

Star System I Processor Module including CPU board, power fail/restart, 4096 x 8 memory and I/O driver board.	3150.00
Additional Core Memory 4096 x 8	1650.00
Base Register Module (for using core memory above 8192 x 8)	450.00
Process Control Language software package (one time charge)	1500.00
Star System I Cabinet including display panel and star System Voltage Regulator	2000.00
Multifunctional Module (MFM)	700.00
Digital Input Module (DIM)	300.00
Digital Output Module (DOM)	300.00
Analog Input Module (AIM)	300.00
Analog Output Module (AOM)	300.00
Peripheral Control Module (PCM)	300.00
Magnetic Tape Controller (MTC)	320.00
Synchronous Modem Controller (SMC)	320.00

STAR SYSTEM AREA DRIVERS AND RECEIVER PRICES

117 V.A.C. Signal Converter 1850-0601	120.00
130 V.D.C. Signal Converter 1850-0631	120.00
117 V.A.C. 1.7 Amp Driver 1850-0636	120.00
130 V.D.C. 1 Amp Driver 1850-0452	120.00
24 V.D.C. 5 Amp Driver 1850-0262	80.00
Analog Input Amplifier 1850-0305	180.00
Slo-Syn Stepper Motor Driver 1850-0151	110.00
Area Module Rack	100.00
15 V.D.C. 2.5 Amp Regulator 1850-0125	100.00

STAR SYSTEM SPECIAL PRODUCT PRICES

Basic 30 CPS Serial Printer PL-30 with Interface to Star System	2395.00
Keyboard Printer PL-31	2545.00
Additional Options:	
With Paper Tape Reader/Punch	1500.00
Mag Tape Cassett Read/Write	1050.00
Card Reader	1750.00
Printer Stand	175.00
Star System Cabinet	350.00

STAR SYSTEM II

PRICES ON REQUEST